**IN THE SPECIFICATION:**

**After line 14, page 8 of the specification, please insert:**

FIG. 28 is a view showing a structural example of a signal line driver circuit shown in FIG. 1 having a plurality of m shift registers, wherein the number of shift registers is a multiple of m.

**Replace the paragraph bridging pages 12 and 13, specifically page 12, line 24 through page 13, line 5, with the following paragraph:**

Although this mode of the invention shows the case where the 3-bit digital picture signal is inputted without division, the digital picture signal to be inputted may be divided to a lower operation frequency of the shift register. In this case, signal transmission lines for 3 bits x division number in total are put, and shift registers, the number of which is equal to that, becomes necessary. Incidentally, the number of DFFs contained in the respective shift registers is decreased correspondingly to the division number. An example of a number of shift registers being a multiple of m (i.e., 3) is shown in FIG. 28.